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None

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UK CL (Edition I) G1G, H4D, H4F
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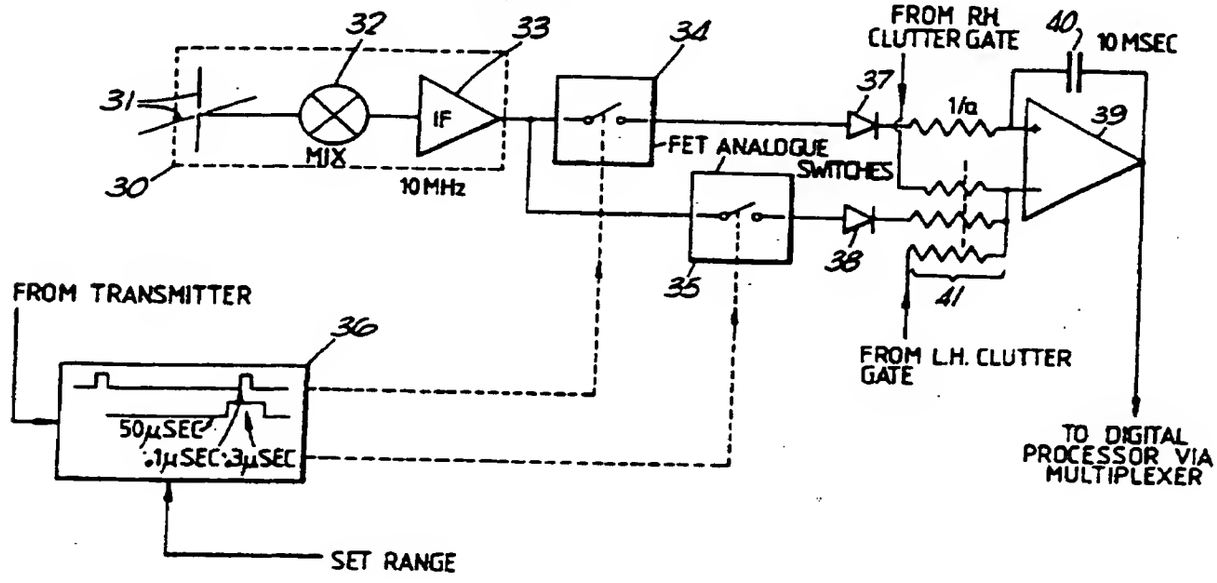
(54) Abstract Title
Target detection

(57) A target detector uses an array of radar receivers for forming respective pixel signals and means for combining signals from adjacent receivers, to provide a 'Laplacian' filtering method for target enhancement. The array is preferably mounted on a dielectric substrate which also carries integrated range gating circuits 34, 35.

Fig. 3.



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

The print reflects an assignment of the application under the provisions of Section 30 of the Patents Act 1977.

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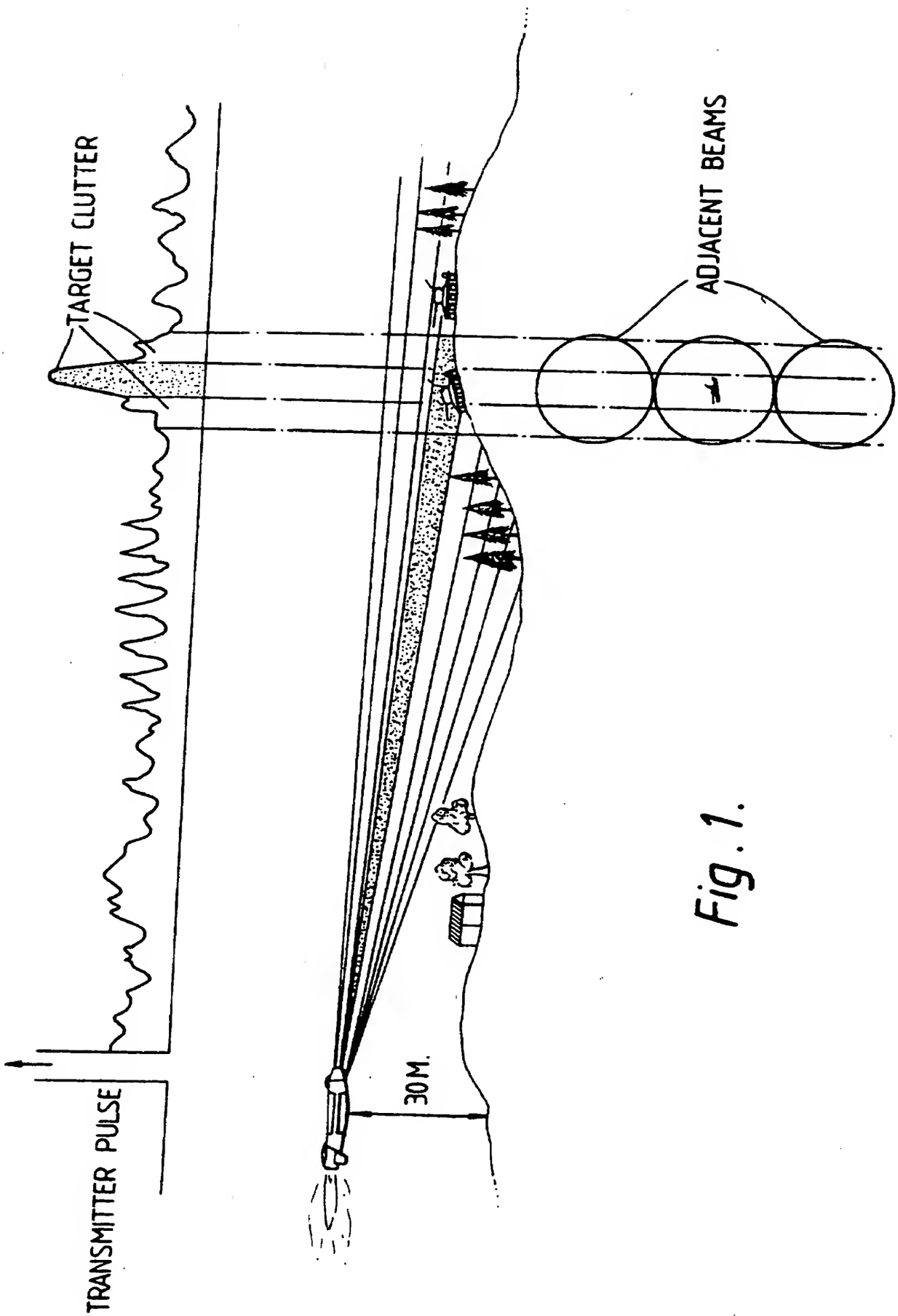

Fig. 1.

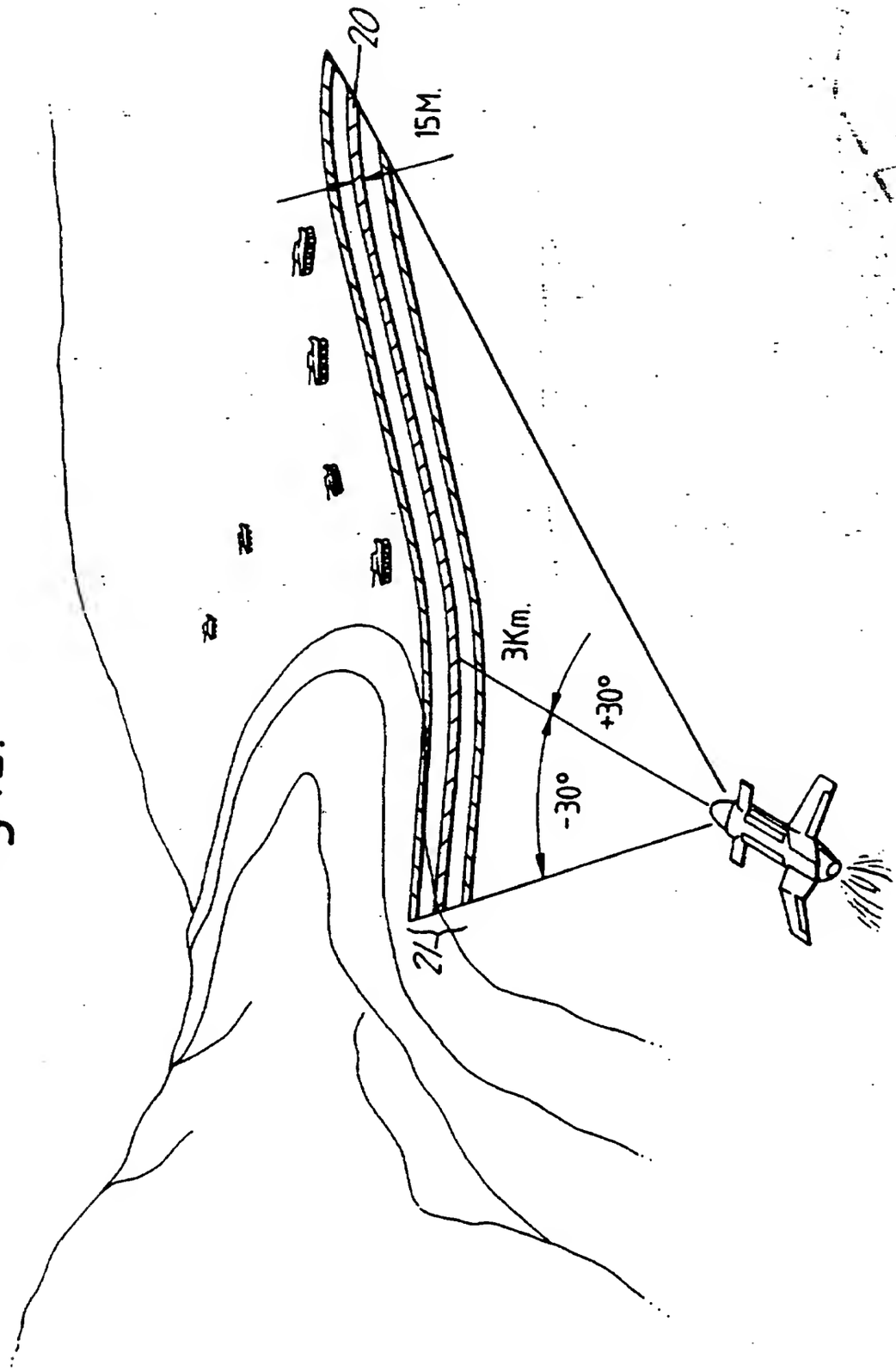

Fig. 2.

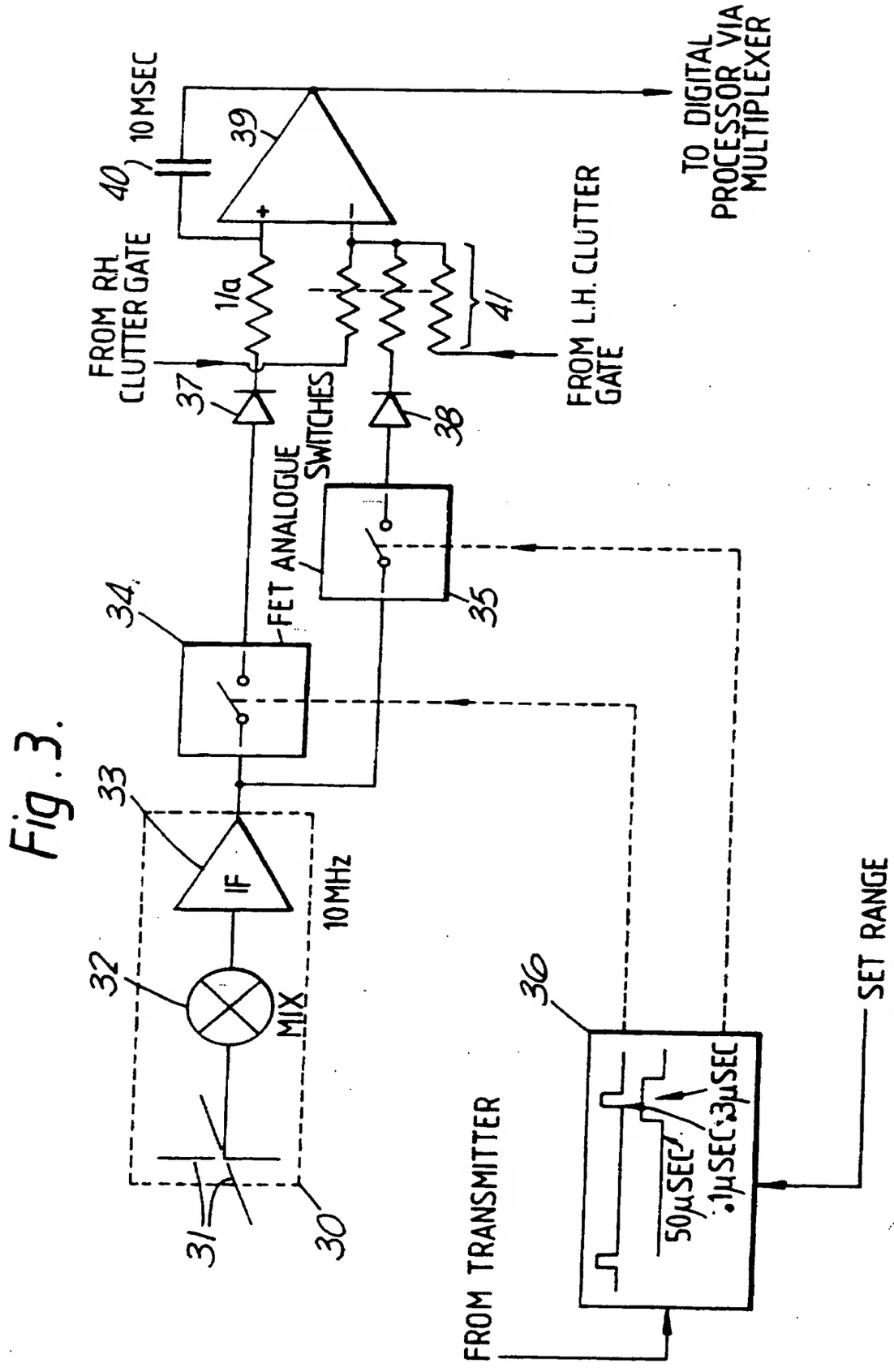
TO DIGITAL PROCESSOR VIA MULTIPLEXER
10 MSEC
40
39
FROM RH CLUTTER GATE
1/a
41
FROM L.H. CLUTTER GATE
37
38
FET ANALOGUE SWITCHES
34
35
33
IF
10MHz
32
MIX
31
30
36
50μSEC
1μSEC
3μSEC
FROM TRANSMITTER
SET RANGE

Fig. 3.

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Target Detection

This invention relates to radar target detection systems of the kind comprising a lens for receiving R.F. radiation returned from a viewed scene and an array of receiver circuits upon which the received radiation is imaged. The scene is thus divided into a series of 'pixels' each of which is viewed by a separate one of the receiver circuits. The system may be of the kind comprising a dielectric lens and, supported at the rear face of a dielectric substrate, an array of integrated antenna/mixer circuits operable to produce respective I.F. signals indicative of the associated 'pixels'. Each circuit may comprise a metallised antenna pattern, for example a pair of crossed dipoles (one to pick up the signal radiation with is arranged to be linearly polarised, and the other to pick up an orthogonally polarised local oscillator radiation, which is directed onto the array) along with a mixer diode arrangement of which the diodes may be integrated into the substrate or applied, in the manner of a thick-film circuit, on top of the metallisation pattern. Various modifications to this basic idea are possible. For example, the metallisation may be such as to define slot antennae rather than dipoles, the local oscillator signal may be injected into the circuits rather than irradiated thereon (i.e. so each circuit need only comprise one dipole but, probably, a more complex structure regarding the attached circuitry), the antennae may be sized for response to harmonics of the signal and/or local oscillator and so on. Such systems are called 'Monolithic Array Receivers'.

When the 'scene' consists of a small target such as a military vehicle viewed against a cluttered background, problems arise of

distinguishing between target and clutter. This is because the radar returns of both may appear to be similar at any receiver output.

A number of methods of distinguishing between a target and clutter have been proposed. These rely on the application of sophisticated data processing to every elementary receiver. Proposed methods include the use of various forms of doppler processing, and the comparison of the target returns at different polarisation planes. All these methods require either the construction of many parallel processing circuits, or the digitisation of the intermediate frequency output from each element and the application of high speed digital processing in series or in parallel to all these outputs. These methods are both expensive and bulky.

One object of the invention is to provide an alternative form of signal processing for target extraction which may be preferred in some cases. A further object is to provide a form of target extraction which can take place on or near the substrate carrying the antenna/mixer circuit array, and thus avoid the above problems of bulky and expensive processing.

According to one aspect of the invention, there is provided a target detection system comprising an array of radar receivers for forming signals indicative of respective pixels of a viewed scene and, for each receiver, signal processing means for combining the receiver output with the outputs of adjacent receivers so as to enhance the contrast between scene items occupying only one pixel as against items extending over several pixels.

According to a second aspect of the invention, there is provided a target detection system comprising an array of radar receivers supported by a dielectric substrate and, for each receiver, range gating means for passing signals from the associated receiver which correspond to radar returns from within a range to the system determined by the range gating means, and integrating means for integrating the signals from the associated receiver, said range gating means and said integrating means being supported by said substrate.

For a better understanding of the invention, reference will be made to the accompanying drawings, in which:-

Figure 1 is a plan view of a missile crossing a terrain and carrying a target detection system;

Figure 2 is a top view corresponding to figure 1; and

Figure 3 is a simplified circuit diagram of part of the detection system used on the figure 1 missile.

The principles involved in this method of processing are illustrated in Figure 1. This shows a plan view of a flying vehicle carrying a monolithic array receiver and searching a scene. The scene is illuminated by a pulse illuminator carried in the vehicle or elsewhere.

In a simple embodiment of this method of processing all the receivers of the array are range gated simultaneously on the chip itself. This ensures that radar returns from only a narrow strip of the scene are received. The strip moves across the scene at the velocity of the flying vehicle, but its position can also be changed by adjusting the range gate. The position of the strip is however independent,

within limits, of the pitch angle of the vehicle and of the undulations of the countryside since it is determined solely by range, see Figure 2. At any instant only receivers which are looking at the scene at the chosen range will have any significant output. All other elements will give an output only of Boltzman noise.

The outputs of all receivers are integrated to enhance the constant between noise on the one hand, and target return plus clutter on the other. In addition, there is incorporated a Laplacian spatial filter into the range gating and integrating process which will have the effect of enhancing targets which occupy only one scene pixel, in contrast to background clutter sources which occupy many such pixels.

An embodiment of this method is illustrated in Figure 3.

Figure 3 shows one receiver 30 from an array of such receivers (the others not being shown) all supported at the back of a dielectric substrate (not shown) which receives signal radiation and local oscillator radiation via a dielectric lens (not shown). The receiver 30 comprises a pair of crossed dipoles 31 interconnected by diodes, represented by mixer symbol 32, and coupled to an IF amplifier 33. The IF output signal of the receiver is passed to each of two range gate switches, and controlled by respective gating pulses from a timing circuit 36. The gating pulses are synchronised by a signal from the transmitter which illuminates the viewed scene and the length and/or position of each is controlled by a set range signal applied to the circuit 36.

The pulses formed by circuit 36 are such as to open gate 34 (called the target gate) for a relatively short time period passing

receiver signals corresponding to returns from within the narrow range band represented by the central shaded band 20 in figure 2 which gate 35 (the clutter gate) is opened for a longer time period, containing the short one, to pass signals corresponding to returns from within the wider band 21 in figure 2.

The IF signals from the target and clutter gates 34 and 35 are detected by diodes 37 and 38 and passed, along with the detected clutter gate outputs from the two adjacent receivers in the array (ie. the receivers looking at portions of the bands 20 and 21 in figure 2 each side of the portion looked at by receiver 30), to a resistor network 41 feeding the sum and difference inputs of a differential amplifier 39 having positive feedback via a capacitor 40 and forming, thereby, an active integrator. The output of the integrator is fed to a digital processing system via a multiplexer (not shown) which multiplexes the outputs of all the integrators into the processing system. The timing circuit 36 may be common to all the receivers or it may be preferred to have one such circuit for each receiver. The gates 34 and 35, detector diodes 37 and 38 resistor network, amplifier 39 and capacitor 40 are supported on the receiver array substrate, say alongside the associated receiver.

Thus, in the illustrated embodiment, two range gates are applied to all the receivers; a 'clutter gate' and a 'target gate'. The clutter gate will be longer than the target gate; in this example the clutter gates are three times its length. Thus if the target gate were 15 metres long the clutter gate would be 45m long. As shown in Figure 3, the output of each elemental receiver has a weighting factor times the

output of its own clutter gate and of the clutter gates of adjacent elements substracted from it. In this instance since 9 x 15m clutter cells are contrasted with each target cell, the weighting factor would be one ninth. The size of the Laplacian filter and its weighting factors would be matched to the average size of the background clutter. If the target is seen against a uniform sea background, for example a much larger number of clutter cells could be used and a greater enhancement of small targets achieved. Other Laplacian filters of this sort can be devised to attentuate known clutter shapes.

As noted, the range gating summation and integration takes place on or near the receiver 30 itself, taking up little more space than the receiver, and leaving only relatively slow speed sampling and picture processing to be performed remote from the receiver array.

The embodiment shown is the simplest envisaged. As will be appreciated, a development would be to employ multiple range gates so that an area may be scanned instead of the line described, though the 'on chip' processing then becomes more complex. By varying the range gate the line can be scanned over the scene, or used to track a target once recognised. In the embodiment shown, the application of a Laplacian filter or similar image processing technique to the multiple outputs of a system of Monolithic Array Receivers is used to enhance the detection of objects which occupy only one pixel compared with larger clutter sources which occupy many pixels. Therein, the use of 'on chip' range gating and integration can reduce the need for a great deal of high speed off chip processing. In addition, by appropriately controlling the range gate timing circuit(s), the same technique of 'on

chip' range gating and integration can be used to produce quasi-picture stabilisation without the need for mechanical gimbals or digital transforms. This stabilisation can be used whether or not the target enhancement processing is carried out.

Claims

1. A target detection system comprising an array of radar receivers for forming signals indicative of respective pixels of a viewed scene and, for each receiver, signal processing means for combining the receiver output with the outputs of adjacent receivers so as to enhance the contrast between scene items occupying only one pixel as against items extending over several pixels.

2. A target detection system comprising an array of radar receivers supported by a dielectric substrate and, for each receiver, range gating means for passing signals from the associated receiver which correspond to radar returns from within a range to the system determined by the range gating means, and integrating means for integrating the signals from the associated receiver, said range gating means and said integrating means being supported by said substrate.

3. A target detection system substantially as hereinbefore described with reference to the accompanying drawings.

Amendments to the claims have been filed as follows

1. A target detection system comprising an array of radar receivers for forming signals indicative of respective pixels of a viewed scene and, for each receiver, signal processing means for combining the receiver output with the outputs of adjacent receivers so as to enhance the contrast between scene items occupying only one pixel as against items extending over several pixels.

2. A target detection system according to Claim 1, the system comprising and array of radar receivers supported by a dielectric substrate and, for each receiver, range gating means for passing signals from the associated receiver, which signals correspond to radar returns from within a range determined by the range gating means, and integrating means for integrating the signals from the associated receiver, said range gating means and said integrating means being supported by said substrate.

3. A target detection system substantially as hereinbefore described with reference to the accompanying drawings.

PATENTS ACT 1977

EXAMINER'S REPORT TO THE COMPTROLLER
UNDER SECTION 17(5)
(The Search Report)

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Application No. 8620091

FIELD OF SEARCH: The search has been conducted through the relevant published UK patent specifications and applications. Applications published under the European Patent Convention and the Patent Co-operation Treaty (and such other documents as are mentioned below) in the following subject-matter areas:-

UK Classification H4D; G1G; H4F

Patent Classifications other than UK, EP & PCT:) Selected US specifications from IPC sub classes H01N G01S

DOCUMENTS IDENTIFIED BY THE EXAMINER (NB In accordance with Section 17(5), the list of documents below may include those considered by the examiner to be the most relevant of those lying within the field (and extent) of search)

	Identity of document and relevant passages	Relevant to claim
	NONE	1

CATEGORY OF CITED DOCUMENTS

X relevant if taken alone
Y relevant if combined with another cited document
P document published on or after the declared priority date but before the filing date of the present application
E patent document published on or after, but with priority date

Search examiner

J BETTS

Date of search

12 March 1987